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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,980	05/25/2000	Jun Yoshida	35.C14505	6464

5514 7590 03/25/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

File

Office Action Summary

Application No.	Applicant(s)	
09/577,980	YOSHIDA ET AL.	
Examiner	**Art Unit**	
Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

0. Applicants's priority paper and IDS of resp. 13 Sept. and 27 July 2000 have been entered. The Examiner has considered the IDS.

0.1 Pursuant to 35 USC 131, **Claims 1-40** are presented for examination.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1.1 **Claims 1-40** are rejected under 35 USC § 112 second paragraph for failing to particularly point out and distinctly define the subject matter which the applicant regards as his invention.

1.1 **As per Claims 1, 11, 21, 31, and intervening claims**: It is not clear to the Examiner how different inputs to a coder/decoder are selectively applied to said coder/decoder so as to process said inputs via a sharing configuration, or how coded/decoded data are selectively separated to be applied to an output means.

1.2 **As per Claims 3-4, 13-14, 23-24, 33-34, and intervening claims**: It is not clear to the Examiner how the parallel process is effected for different inputs to a coder/decoder or the design requirement for encoding same inputs via parallel means to result in processing bottleneck wherein it is not possible to differentiate coded/decoded results from a 1st parallel operation from a 2nd parallel operation.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2.1 **Claims 11-20** and **31-40** are rejected under 35 U.S.C. 101 as claiming a mathematical formula or algorithm. Applicant is advised to modify limitations of said claims as being incorporated or embedded in hardware or readable machine medium.

Claim Objections

3. **Claim 2, 4, 7, 12, 14, 17, 22, 24, 32** and **34** are objected to under 37 CFR 1.75 because 'Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP 608.01(i)- (p).'

Claims 11, 31 are objected to because they recite 'step of [for] encoding/decoding'.

Appropriate correction is required.

Claim Rejections - 35 USC ' 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4.1 **Claims 1-40** are rejected under 35 U.S.C. 102 (e) as being anticipated by **Kobayashi et al.** (US Patent No. 6,029,264; April 28, 1997).

As per Claims 1-40, Kobayashi et al. discloses algorithm means to select from a plurality of encoding/decoding algorithms based on computation needs of a user at col. 4 line 30 et seq., e.g., in Fig. 12C below an equivalent turbo/convolutional/concatenated/parallel concatenated system comprising: maximum likelihood decoder, 1st error detector/corrector, a code demodulator, and a second error detector/corrector, digital modulation means, code or block dividing or partitioning (Fig. 5), permutation or interleaving for burst error reduction; means for post coder for partial response in col. 2 line 21; means for cyclically coded bit in col. 6

line 40; means for detecting and correcting errors based on predetermined parameters such as number of errors, e.g., "*if the received sequence does not satisfy parity-check equations, then the receiver detects the existence of some errors and, in some cases, can correct them.*" in col. 1 lines 39-et seq.;

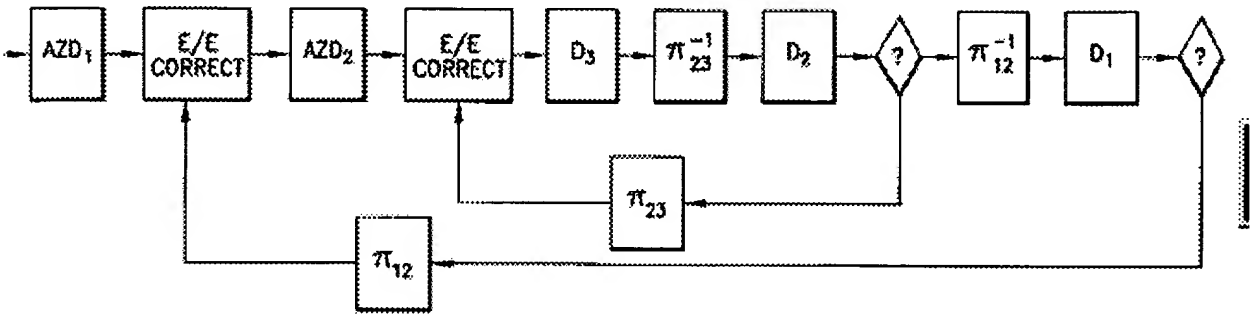

FIG.12C

means for run-length limiting coding, e.g., "*digital recording, is run-length limited codes, denoted (d,k)-limited codes. The integer parameters d and k represent the minimum and maximum numbers of runs of either 0's or 1's that are allowed in the encoded sequence. The lower bound d is chosen from the ISI consideration, and the upper bound k is set to insure clock synchronization capability at the receiver side*," in col. 2 lines 39-46; and for means for cyclically coding bits in col. 6 line 40.

4.2 **Claims 1-40** are rejected under 35 U.S.C. 102(e) as being anticipated by **Ott** (US Patent No. 6,182,264; May 22, 1998).

As per Claims 1-40, Ott teaches an equivalent routine in col. 1 line 5 – col. 11 line 64 wherein a processor, **sharing a common EDC** in e.g., Fig. 1: Block 117, is configured to dynamically select one of plural error correction processes/techniques based on measured transmission channel error rates or channel conditions so as to reduce power consumption or circuit hardware or both, e.g., when error rate is in a low or high state such that power consumed while processing one of plural error correction codes corresponds to an appropriate error rate as

depicted by Figs. 1-4.

Ott discloses means for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1: block 101), a data transmitter (Fig. 1: block 118), and means for performing a plurality of error detection and/or correction techniques said method comprising: receiving data having a given EDC coding;

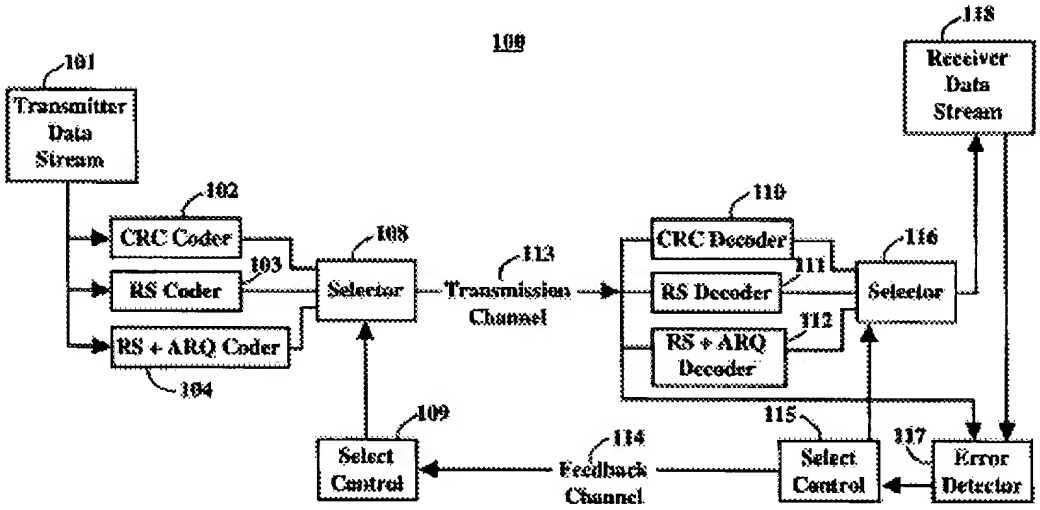

FIG. 1

determining an error rate (Fig. 4: block 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques; comparing said error rate to at least one error threshold value; and selecting (Fig. 4: block selects 408 and 404) one of said plurality of error detection and/or correction techniques of said electronic device based on an outcome of said comparing step (Fig. 4: block compares 407 and 402-403); determining an error rate (Fig. 4: block decision 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques (Fig. 4: block selects 408 and 404). Examiner notes that it is clear to those of ordinary skill in data communications that error detection generally requires

less hardware that error correction and that less energy is consumed/required for error detection processing than for error correction because less signal processing is performed in detection.

Ott also discloses procedure wherein error threshold value corresponds to an error rate which will ensure that said selected error detection and/or correction technique is one which consumes a lowest amount of power while maintaining a desired signal-to noise ratio in Fig. 4;

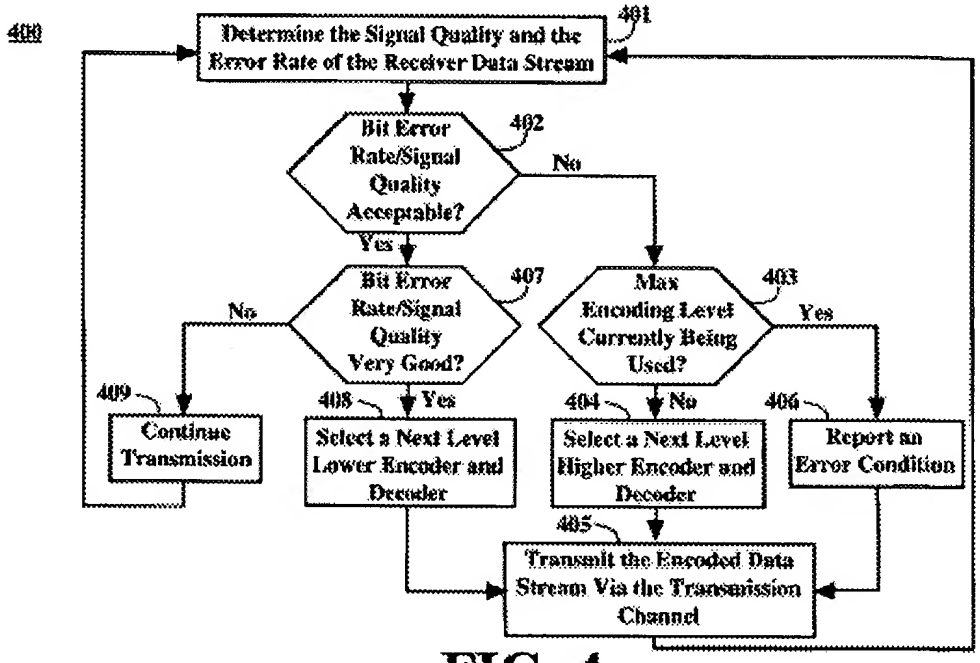

FIG. 4

wherein if said error rate is below said error threshold value, said selecting step includes: selecting an error detection and/or correction technique which is less complex and consumes less power than said initial error detection and/or correction circuit **in Fig. 4**.; wherein if said error rate exceeds said error threshold value, said selecting step includes: selecting an error detection and/or correction technique which is more complex and consumes more power than said initial error detection and/or correction circuit **in Fig. 4; and** further comprising: means for adjusting at least one controller operating parameter to support performance of said selected error detection and/or correction technique **in Fig. 4; and** further comprising: adjusting an output signal level of

said data transmitter in accordance with an outcome of said comparing step **in Fig. 4**; and whereby a user or a controller provides an external signal or signal to enable selection of error detection and/or correction technique in accordance with said external signal or signal, said operation being used for power level compensation **in Fig. 4**.; wherein said external signal causes an error detection and/or correction technique having a higher complexity and power consumption level than said initial error detection and/or correct technique, said external signal thereby improving signal-to-noise ratio at an expense of increased power consumption **in Fig. 4**; and wherein said external signal causes an error detection and/or correction technique having a lower complexity and power consumption level than said initial error detection and/or correct technique, said external signal thereby improving power consumption at an expense of a lower signal-to-noise ratio **in Fig. 4;** and wherein said plurality of error detection and/or correction techniques is at least three, and wherein said comparing step includes: comparing said error rate to a first error threshold value, and if said error rate is less than said first error rate, selecting an error detection and/or correction technique of low complexity and power consumption requirements; if said error rate is greater than said first error rate but lower than a second error threshold value, selecting an error detection and/or correct technique of medium complexity and power consumption requirements; and if said error rate is greater than said second error threshold value, selecting an error detection and/or correction technique of high complexity and power consumption requirements **in Fig. 4**.

Ott further discloses, in Figs. 1 and 4, an algorithm for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1), a data transmitter (Fig. 1), and means for performing a plurality of error detection and/or correction techniques (Fig. 1: blocks 102-104 and 110-112), said method comprising: receiving an external or manually or automatically entered signal from a user; and selecting one of a plurality of error detection and/or

correction techniques in accordance with said external signal, said plurality of error detection and/or correction techniques consuming different levels of power and having different levels of complexity; wherein said external signal causes an error detection and/or correction technique which is one of the following: an error detection and/or correction technique (cols. 4-5: **crc or rs or turbo or convolutional coding, etc**) having a higher complexity and power consumption level than a currently selected error detection and/or correct technique, said external signal thereby improving signal-to-noise ratio at an expense of increased power consumption; and an error detection and/or correction technique having a lower complexity and power consumption level than said currently selected error detection and/or correct technique, said external signal thereby improving power consumption at an expense of a lower signal-to-noise ratio **and** whereby a user or a controller provides an external signal or signal to enable selection of error detection and/or correction technique in accordance with said external signal or signal, said operation being used for power level compensation **in Fig. 4**.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.0 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5.1 **Claims 1-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ott** (US Patent No. 6,182,264; May 22, 1998) in view of **Kobayashi** (US Patent No. 6,029,264; 28 Apr. 1997).

As per Claims 1-40, Ott substantially discloses data processing means, in col. 1 line 5 –

col. 11 line 64, wherein a processor is configured to dynamically select one of plural error correction processes/techniques/algorithms based on measured transmission channel error rates or channel conditions so as to reduce power consumption or circuit hardware or both, e.g., when error rate is in a low or high state such that power consumed while processing one of plural error correction codes corresponds to an appropriate error rate as depicted by Figs. 1-4.

Ott also discloses means for controlling power consumption in an electronic device, said device including a data receiver (Fig. 1: block 101), a data transmitter (Fig. 1: block 118), and means for performing a plurality of error detection and/or correction techniques said method comprising: receiving data having a given EDC coding; means for **sharing a common EDC** in e.g., Fig. 1: Block 117

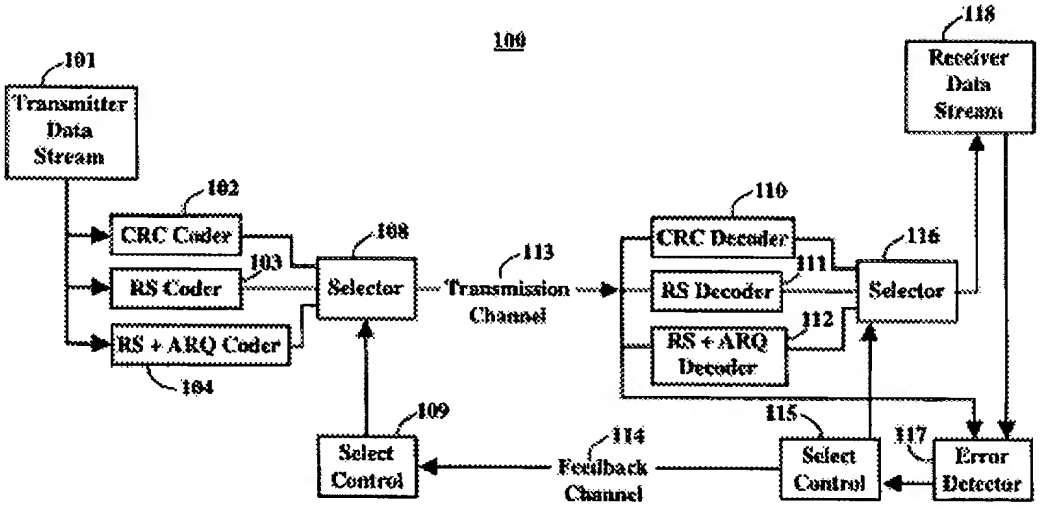

FIG. 1

determining an error rate (Fig. 4: block 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques; comparing said error rate to at least one error threshold value; and **selecting** (Fig. 4: block selects 408 and 404) **one of said plurality of error detection and/or correction**

techniques/ALGORITHMS of said electronic device based on an outcome of said comparing step (Fig. 4: block compares 407 and 402-403); determining an error rate (Fig. 4: block decision 401) corresponding to said received data, said error rate being determined by an initial one of said plurality of error detection and/or correction techniques (Fig. 4: block selects 408 and 404).

Ott also discloses a procedure wherein said error threshold value corresponds to an error rate which will ensure that said selected error detection and/or correction technique is one which consumes a lowest amount of power while maintaining a desired signal-to noise ratio in Fig. 4.

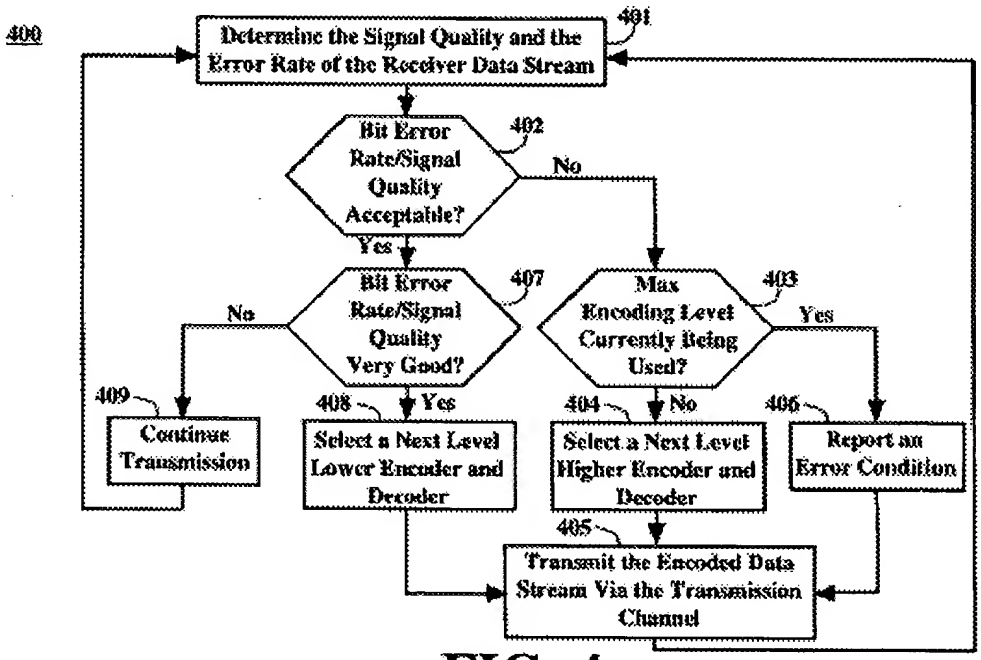

FIG. 4

Not specifically described in detail by **Ott** is the step whereby the selected algorithm is also effected using mathematical formulation via convolutional or turbo coding along with interleaving/RLL means.

However Kobayashi et al., in an analogous art, discloses algorithm means wherein such technique is performed. {See **Kobayashi**, Id., for algorithm switching means to select one ECC codec algorithm out of a plurality of encoding/decoding algorithms based on computation needs

of a user at col. 4 line 30 et seq. and Figs. 1-14}. **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the process of **Ott** by including therein the technique of substituting ECC means *such as turbo/convolutional/RLL/CRC/RS codes* as disclosed by **Kobayashi** because such modification would provide the procedure of **Ott** with a method whereby *"a variety of ECC, such as turbo/convolutional/RLL/CRC/RS codes, may be implemented based on channel conditions, inter allia, so as to optimize data processing for reduction either in power consumption or hardware overhead or both."* {See **Kobayashi**, Id., e.g., col. 3 line 36.}

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Patent Examiner
3/21/04